RZ/G Series, 2nd Generation

DQ Timing Margin Checker User's Manual

Introduction

This document describes the information of DQ timing margin checker (hereinafter, this is called DQ margin checker) and how to use it whose ex-name is EYE opening tool. The DQ margin checker simply provides setup and hold timing margin between DQS and each DQ signals.

Note that this tool doesn't provide functions for setting DRAM parameters. Therefore, this tool must be built for each DRAM settings.

This tool is based on the Flash Writer published on GitHub. You can add this tool as a command to the Flash Writer and build with customized DRAM setting you like.

CAUTION

Don't disclose source code provided in the patch file to anyone other than related person.

Target Device

RZ/G2L, G2LC, G2UL, V2L

Contents

1. Overview

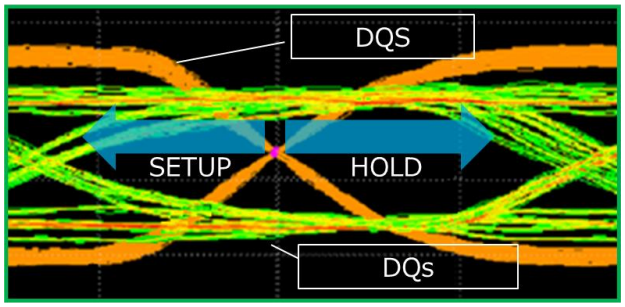
The DQ margin checker provides the setup and hold margin between DQS and each DQ signals by sweeping SoC internal delay. Both read and write DQ access margin will be measured.

Data accesses are made by burst data transfer with DMA.

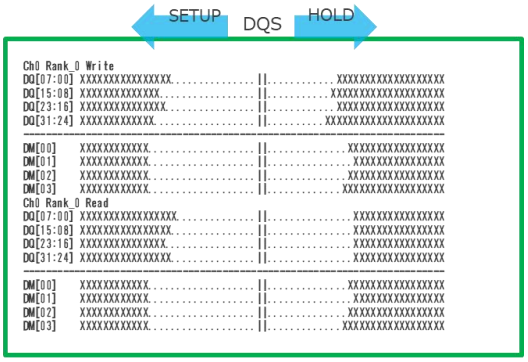
Note that this tool only supports the SCIF boot mode. Therefore, the target board must have connectors or terminals for connection to PC via SCIF.

Also note that this tool does not provide to change DRAM setting. Therefore, software build for each DRAM settings are needed.

Customizing DRAM setting is provided with “DDR config generation tool”. If you don’t have it, please ask Renesas.



Actual waveform image



Report Image

2. Getting Started

This tool provides visualized DQ to DQS setup/hold margin of DRAMs implemented on your board. This tool works on a target device only in SCIF download mode, thus it will be controlled with terminal application software on a PC. In this document, we use Tera Term as terminal software for example.

2.1 [optional] Build ARM toolchain

If this is first build with ARM toolchain, it is needed to build ARM toolchain as following commands for example:

```
$ cd ~/
$ wget https://developer.arm.com/-/media/Files/downloads/gnu-a/10.2-2020.11/binrel/gcc-arm-10.2-2020.11-x86_64-aarch64-none-elf.tar.xz
$ tar xvf gcc-arm-10.2-2020.11-x86_64-aarch64-none-elf.tar.xz
```

NOTE

See also “RZ/G2L, RZ/G2LC and RZ/V2L SMARC EVK Start-up Guide” for more detail.

2.2 Build DQ margin checker

The DQ margin checker is based on the Flash Writer published on GitHub. Then you need to clone it to your development environment and apply the patch file provided from us.

GitHub - renesas-rz/rzg2_flash_writer

```
$ cd ~/
$ git clone https://github.com/renesas-rz/rzg2_flash_writer.git
$ cd rzg2_flash_writer
$ git checkout 457f62c
$ git apply dq_margin_checker.patch
$ make clean
$ make BOARD=<board> EMMC=0
```

Target board	BOARD option
RZ/G2L Evaluation Board Kit	RZG2L_SMARC_PMIC
RZ/G2LC Evaluation Board Kit	RZG2LC_SMARC_PMIC
RZ/V2L Evaluation Board Kit	RZV2L_SMARC_PMIC
RZ/G2UL Evaluation Board Kit	RZG2UL_SMARC

Using other board setting excluding the above, see 3.Adapting Original DRAM Setting.

2.3 Hardware and Software Setting

A) Install Tera Term into your PC.

B) Connect the board and the PC with a USB cable.

C) Set the target device on your board to SCIF download mode. If you are using a Renesas’ board, set DIP switches on the board. Please refer to its user’s manual.

D) Launch the Tera Term and select “Serial” for communication method and an appropriate COM port connected to the board.

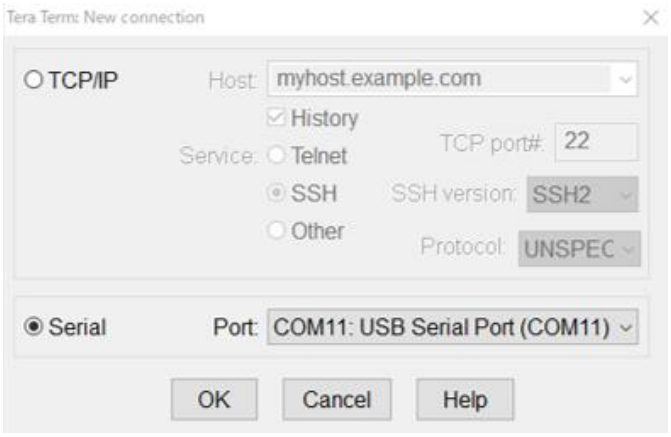


Figure 1 Select New Connection

E) Configure serial port setting as following (Select 'Setup' menu -> 'Serial port').

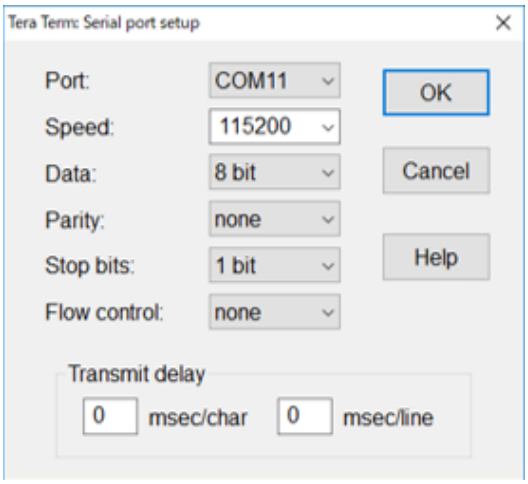


Figure 2 Serial Port Setup

F) Turn on your board. Then you can look SCIF download mode message.

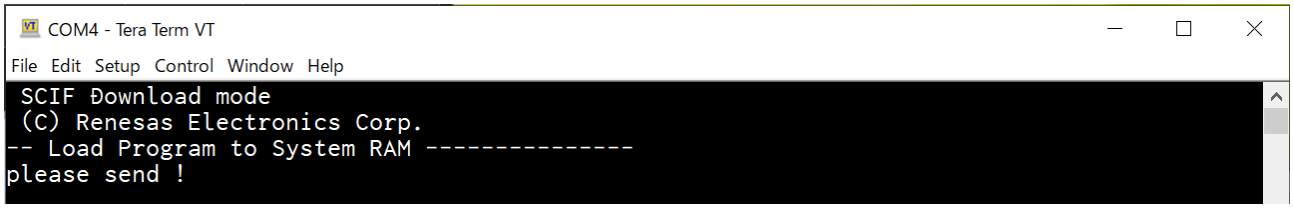


Figure 3 Power ON Message

G) Send the s-record format file (Select "File" menu -> "Send file")

H) After the download finished, the prompt ">" will appear. It's ready to start DQ margin checker.

NOTE

In SCIF download mode, the program file is located on SRAM on the target device, thus the program is volatile. You need to send the file again when you reset the device.

2.4 Run Program

Enter “DQ” command to start the DQ margin checker. After the test program finished, the test result will be output on the terminal.

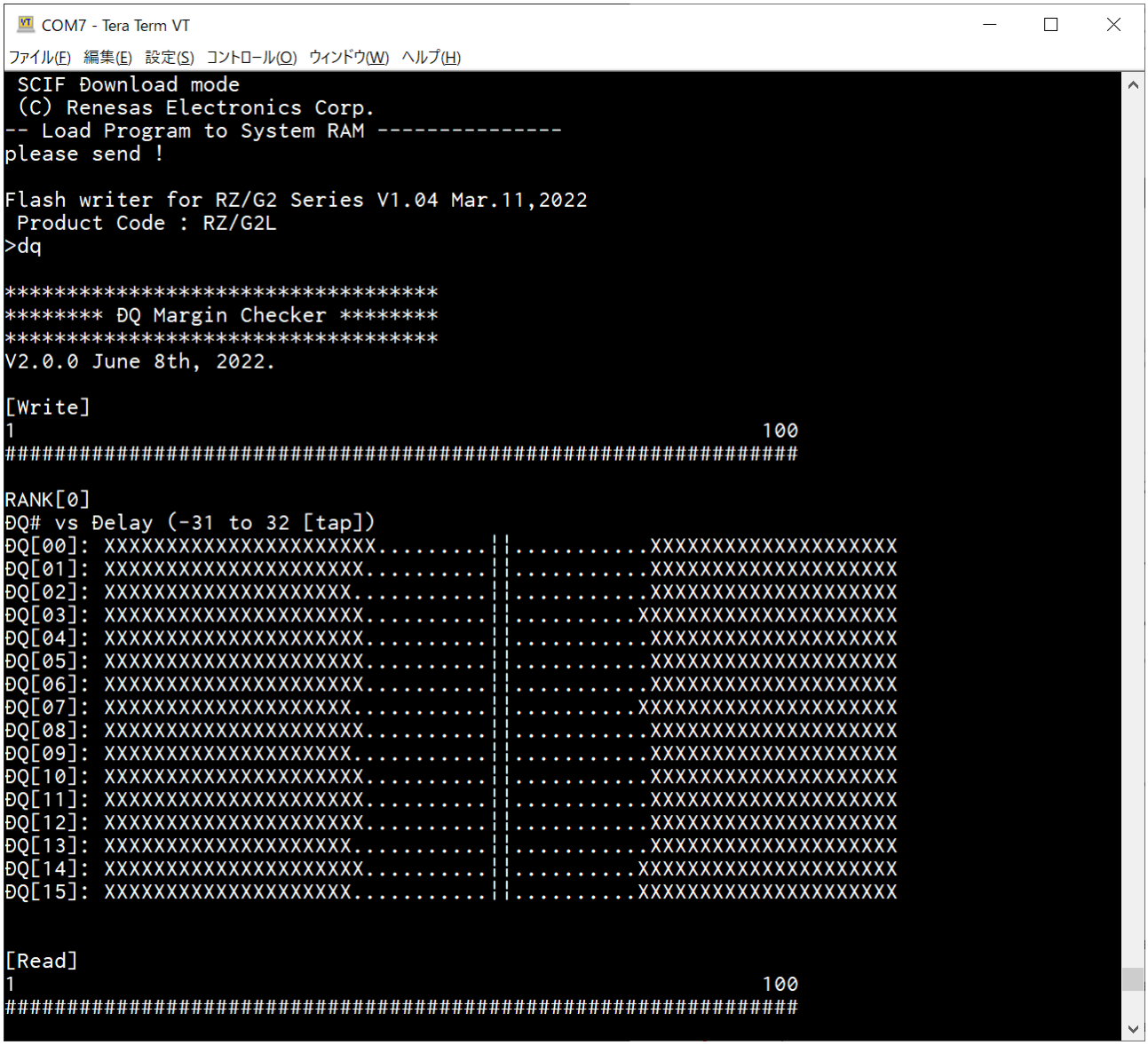


Figure 4 Output example

3. Adapting Original DRAM Setting

If you want to adapt original DRAM setting to this tool, following procedure is needed:

- Generate two files (param_mc.c and param_swizzle.c) with the “DDR configuration generation tool” .xlsm file.
- Copy param_swizzle.c in the ddr/common folder and param_mc.c in the ddr/g2l (or other SoC) folder.

4. Understanding The Result

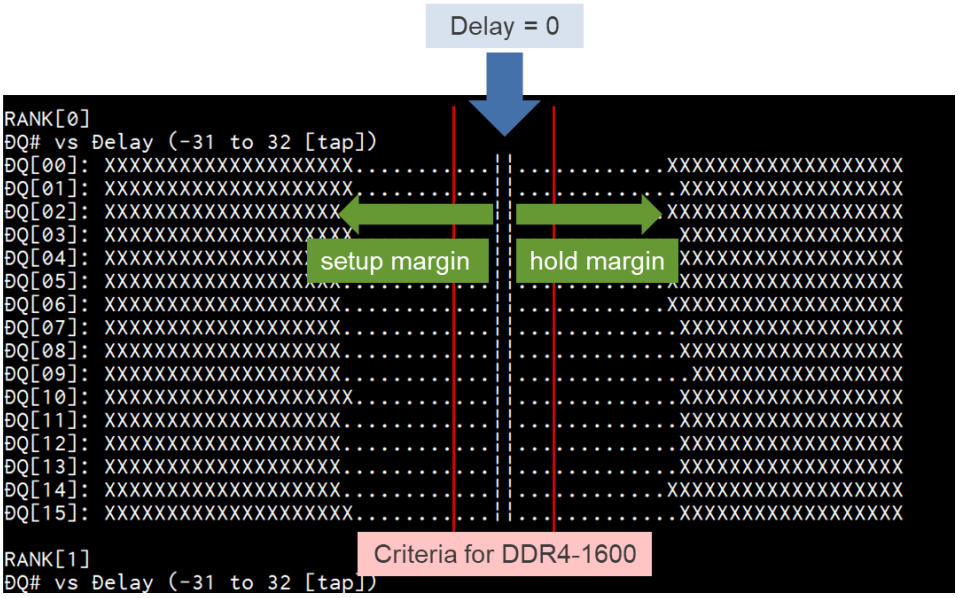
The “.” means that the write and read comparison check was passed, and the “X” means failed. Thus, the dots on left side of the center bar means setup margin, and ones on right side means hold margin.

In the case of speed bin DDR4-1600, a dot represents about 21.6ps(=1250ps/58). The following figure depicts an example of result. Its setup and hold timing margin of DQ0 in the first line are 237ps and 257ps, which equal to 11dots and 12dots, respectively. Therefore, this result means timing margin is enough.

4.1 Criteria on JEDEC Standard

The JEDEC 79-4 standard for DDR4 defines the DQ input receiver compliance mask for voltage and timing. For example, 0.2UI timing margin and 136mV voltage margin are required for DDR4-1600. A 1UI equals to 625ps(=1/800MHz/2) in this case, thus 0.2UI equals 125ps and +/-3 dots(>125ps/21.6ps) in the result are enough for the timing margin.

Note that the Rx mask is defined for stipulated waveforms called eye pattern at balls on each DRAM component, while the DQ margin checker outputs result of comparison write and read data. To be precise, target spec of the Rx mask and result of this checker are different.



5. Data Pattern

The data pattern is fixed to PRBS patterns generated in DDRTOP APN for internal.

6. Appendix: Result of EVK

6.1 RZ/G2L

```
Flash writer for RZ/G2 Series V1.04 Mar.11,2022
 Product Code : RZ/G2L
>dq

**********************************
******** DQ Margin Checker ********
**********************************
V2.0.0 June 8th, 2022.

[Write]
1                                                              100
################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXX...........||..........XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXX...........||..........XXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX...........||..........XXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX

RANK[1]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
```

```
DQ[04]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXX...........||..........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXX


[Read]
1                                                              100
######################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX

RANK[1]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXX
```

```
DQ[03]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXXX........||.........XXXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX

FINISH!
```

6.2 RZ/G2LC

```
Flash writer for RZ/G2 Series V1.04 Mar.11,2022
 Product Code : RZ/G2LC
>dq

**********************************
******** DQ Margin Checker ********
**********************************
V2.0.0 June 8th, 2022.

[Write]
1                                                                  100
######################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXXX.........||............XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX


[Read]
1                                                                  100
######################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
```

```
DQ[01]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXXX........||........XXXXXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXXX........||........XXXXXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXXX........||........XXXXXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX

FINISH!
```

6.3 RZ/V2L

```
Flash writer for RZ/V2 Series V1.04 Mar.11,2022
 Product Code : RZ/V2L
>dq

**********************************
******** DQ Margin Checker ********
**********************************
V2.0.0 June 8th, 2022.

[Write]
1                                                                  100
########################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXXX.........||.............XXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX..........||...........XXXXXXXXXXXXXXXXXX

RANK[1]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXXX.........||.............XXXXXXXXXXXXXXXXX
```

```
DQ[06]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX.........||...........XXXXXXXXXXXXXXXXXX


[Read]
1                                                              100
######################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX

RANK[1]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
```

```
DQ[05]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXXX........||.........XXXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXX..........||.......XXXXXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX

FINISH!
```

6.4 RZ/G2UL

```
Flash writer for RZ/G2 Series V1.04 Mar.11,2022
 Product Code : RZ/G2UL Type1
>dq

*********************************
******** DQ Margin Checker ********
*********************************
V2.0.0 June 8th, 2022.

[Write]
1                                                                  100
#####################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[01]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX..........||............XXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX...........||...........XXXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXX............||............XXXXXXXXXXXXXXXXXX


[Read]
1                                                                  100
#####################################################################

RANK[0]
DQ# vs Delay (-31 to 32 [tap])
DQ[00]: XXXXXXXXXXXXXXXXXXX...........||........XXXXXXXXXXXXXXXXXXXXXX
```

```
DQ[01]: XXXXXXXXXXXXXXXXXXXX.........||..........XXXXXXXXXXXXXXXXXXX
DQ[02]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[03]: XXXXXXXXXXXXXXXXXXXXX........||..........XXXXXXXXXXXXXXXXXXX
DQ[04]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[05]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[06]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[07]: XXXXXXXXXXXXXXXXXXXX.........||........XXXXXXXXXXXXXXXXXXXXX
DQ[08]: XXXXXXXXXXXXXXXXXXX..........||........XXXXXXXXXXXXXXXXXXXXX
DQ[09]: XXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[10]: XXXXXXXXXXXXXXXXXXXX.........||.........XXXXXXXXXXXXXXXXXXXX
DQ[11]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[12]: XXXXXXXXXXXXXXXXXXX..........||..........XXXXXXXXXXXXXXXXXXX
DQ[13]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[14]: XXXXXXXXXXXXXXXXXXX..........||.........XXXXXXXXXXXXXXXXXXXX
DQ[15]: XXXXXXXXXXXXXXXXXXX..........||.......XXXXXXXXXXXXXXXXXXXXXX

FINISH!
```

Revision History

Ver.	Date	Description	
		Page	Summary
1.00	Mar. 11th, 2022.	-	First issued.
1.01	Mar. 31st, 2022.	2, 6	Fixed Overview and command description.
2.00	June 8th, 2022.	all	Fixed with the update to DQ margin checker v2.0.0.
2.1.0	July 14, 2022	7, 8-17	Added section 4.1 and chapter 6.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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